Updated: March 8, 2017

Spring 2017 – Class Schedule Electrical & Computer Engineering

Timing	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
6:00pm 7:30pm	Parallel and Distributed Computing *(CE-Dig. Design & Arch.)*	--	Parallel and Distributed Computing *(CE-Dig. Design & Arch.)*	Digital Processing of Speech Signals *(EE-Signal Processing)*	Data Mining *(CE-Dig. Design & Arch.)*	Linear Systems & Controls *(EE-Control)*
Classroom	***F-03***	***-***	***F-03***	***F-03***	***B-03***	***F-03***
7:30pm 9:00pm	Digital Processing of Speech Signals *(EE-Signal Processing)*	Optimization Techniques *(Mino-/Mathematics)*	--	Optimization Techniques *(Minor-Mathematics)*	Data Mining *(CE-Dig. Design & Arch.)*	Linear Systems & Controls *(EE-Control)*
Classroom	***F-03***	***F-03***	***-***	***F-03***	***B-03***	***F-03***

Timing	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
6:00pm 7:30pm	Power Systems Engineering *(EE-Electrical Energy)*	Cryptography & Network Security *(CE-Information Security/CE-Networks)*	Power Systems Engineering *(EE-Electrical Energy)*	Cryptography & Network Security *(CE-Information Security/CE-Networks)*	Adhoc & Sensor Networks *(CE-Networks)*	--
Classroom	***F-02***	***F-02***	***F-02***	***F-02***	***F-02***	***-***
7:30pm 9:00pm	--	Real Time Embedded Systems *(CE-Dig. Design & Arch.)*	--	Real Time Embedded Systems *(CE/Dig. Design & Arch.)*	Adhoc & Sensor Networks *(CE-Networks)*	--
Classroom	***-***	***F-02***	***-***	***F-02***	***F-02***	***-***

Timing	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
6:00pm 7:30pm	Advanced Digital Signal Processing *(EE/Signal Processing)*	--	Advanced Digital Signal Processing *(EE-Signal Processing)*	--	--	--
Classroom	***B-02***	***-***	***B-02***	***-***	***-***	***-***
7:30pm 9:00pm	--	--	--	--	--	--
Classroom	***-***	***-***	***-***	***-***	***-***	***-***

1. ***The course schedule is subject to change at any time without any prior notice by the CASE Management.***
2. ***CASE has the right to cancel any course if the number of registration falls below a pre-established level.***
3. ***Students are not allowed to register for courses with conflicting schedules.***
4. ***PhD Students are not allowed to register the course of Real Time Embedded Systems.***